REMARKS

Applicants acknowledge receipt of the Examiner's Office Action dated April 29, 2005. Claims 1-22 are currently pending in this application. The Examiner allowed, with thanks, claims 1-19. Claims 20-22 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,377,182 issued to Monacos ("Monacos") in view of U.S. Patent No. 6,178,171, issued to Alexander, Jr. et al. ("Alexander"). In light of the foregoing amendments and following remarks, Applicants respectfully request the Examiner's reconsideration and reexamination of claims 20-22.

Independent claim 20 recites:

> A method comprising:
> a memory circuit receiving a data frame to be transmitted to a destination device via a switching fabric, wherein the switching fabric comprises a plurality of data ports through which data frames enter or exit the switching fabric, wherein the memory circuit is coupled to the switching fabric via **a first pair of the plurality of data ports**;
> generating and adding routing data to the data frame received by the memory circuit, wherein the routing data identifies one of the plurality of data ports through which the data frame will exit the switching fabric to reach the destination device;
> the memory circuit transmitting the received data frame to the switching fabric after the routing data is added to the data frame.

Claim 20 requires a memory circuit that is coupled to the switching fabric via **a first pair of the plurality of data ports**. The Office Action does not clearly state where in Monacos this limitation of independent claim 20 can be found. The Office Action indicates the Abstract, column 16; lines 43-54, column 2; lines 10-35, and Figure 12 of Monacos discloses all the limitations of claim 20 with the exception of generating and adding routing data to the date frame

received by the memory circuit. As an aside, it is noted that column 2, lines 10-35 appear identical to the Abstract.

Applicants have reviewed the Abstract, column 16; lines 43-54, and Figure 12 of Monacos and can find no teaching or fair suggestion of a memory circuit coupled to the switching fabric **via a first pair of data ports** as required by independent claim 20, either alone or in combination with the remaining limitations of independent claim 20. Monacos' Abstract teaches an NxN crossbar for routing packets, each packet having a header identifying one of the output ports of the NxN crossbar as its destination. The NxN crossbar consists of a plurality of switches. An exemplary switch is shown within Figure 12 of Monacos. While the NxN crossbar may be equivalent to claim 20's switching fabric, neither the Abstract or column 16, lines 43-54 of Monacos discloses a memory circuit coupled to the NxN crossbar via **a first pair of data ports**.

At best, Figure 12 cited in the Office Action discloses a 2x2 switching element coupled to a header detector. The header detector in turn includes two instances of header detection logic. The 2x2 switching element may be equivalent to claim 20's switching fabric. For purposes of this Office Action only, Applicants will assume that each instance of the header detection logic within Figure 12 receives and stores a packet or a packet containing a data frame. Figure 12 shows that there are two connections between each header detection logic and the 2x2 switching element. One of these connections is shown transmitting HDET. A review of Monacos shows that HDET stands for header detection signal. **Only one of the two connections between the header logic and the 2x2 switching logic transmits data frames**.

Figure 12 does not show either header detection logic (equated for the purposes of this Office Action with claim 20's memory circuit) coupled to the 2x2 switching element via a pair of data ports. Rather, each instance of the header detection logic is coupled to the 2x2 switching

element by at most, one data port and one header detection signal line. Accordingly, Figure 12 does not teach or fairly suggest a memory circuit receiving a data frame to be transmitted to a destination device via switching fabric, wherein the memory circuit is coupled to the switching fabric via first pair of data ports, either alone or in combination with the other limitations of claim 20.

The Office Action asserts that it would have been obvious to provide the means and step of generating and adding routing data to the data frame received by the memory circuit as taught by Alexander in the communication apparatus and method of Monacos. Applicants reserve the right to contest the combination of Monacos and Alexander to reject claims 20-22 under 35 U.S.C. § 103.

Independent claims 21 and 22 recite limitations similar to that of independent claim 20. Specifically, independent claim 21 recites "transmitting the received data frame to the switching fabric via one of **two data ports coupled to the computer system**" and independent claim 22 recites "wherein the buffer is coupled to the switching fabric via **first and second data ports of the plurality of data ports**." Based upon the arguments made above with respect with to independent claim 20, Applicants assert that the cited sections of Monacos does not teach or fairly suggest the aforementioned limitations of independent claims 21 and 22, either alone or in combination with the remaining limitations of independent claims 21 and 22. Accordingly, Applicants assert that independent claims 21 and 22 are patentably distinguishable over the combination of Monacos and Alexander.

It is noted that independent claim 21 was amended to correct a minor error. Applicants submit that this amendment to independent claim 21 does not require further search or consideration. Indeed it appears that the Office Action treats independent claim 21 as if the correction made herein is understood.

CONCLUSION

Applicants submit that all claims are now in condition for allowance, and an early notice to that effect is earnestly solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia, 22313-1450, on 7/1/05.

Attorney for Applicant(s) — Date of Signature 7/1/05

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